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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,810	01/27/2004	Ravindraraj Ramaraju	SC13162TC	2467

23125 7590 12/23/2004

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,810	RAMARAJU, RAVINDRARAJ	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☒ Claim(s) *1 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 01/27/2004 is acceptable.

Claim Objections

2. **Claims 1 and 22** are objected to because of the following informalities:

- **Claim 1** recites on line 27: "the second conductive line between the first and second conductive lines", which should be "the second conductive line between the first and **third** conductive lines".

- **Claim 1** recites: "a first direction", **claim 22**, dependent upon claim 1, also recites "a first direction" (page 18, line 1). The "a first direction" of claim 22 should be "the first direction".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-21 and 23-29** are rejected under 35 U.S.C. 102(e) as being anticipated by Buffet et al. U.S. Patent 6,586,828.

Buffet discloses in the figures, particularly Figs. 5 and 6, and respective portions of the specification an integrated circuit as claimed. In particular, Buffet discloses a grid for a power supply distribution of cells of circuits having a plurality of sub-grids ("repeatable grid" 106, Figs. 5-6 and column 4, line 46+) in which each sub-grid has continuous lines across it. Each line has an unchanging width but the widths of the lines vary from each other. The lines on the perimeter are the thickest and each line is thinner than the previous line until the middle is reached (most clearly seen from Fig. 5 and disclosed in more details in column 4, lines 30-35, column 6, first paragraph, and tables I and II). Thus, the line or lines in the middle are the thinnest.

More particular, in reference to **claim 1**, for being consistent with claim terminology, if one labels, from Fig. 6, the center line 30' as a third conductive line, the outermost lines 30' as a first and fifth conductive lines, and any of the conductive line 30' between the center line and the first and fifth conductive lines as a second and a fourth conductive lines, one obtains an integrated circuit comprising:

a substrate (24, Fig. 2) including active circuitry;

an interconnect (M1-M7) overlying the substrate; and

a conductive grid (106, Fig. 6), the conductive grid including a plurality of conductive lines located in a first interconnect layer of the interconnect, each of the plurality of conductive lines extending across at least a majority of the integrated circuit in the first interconnect layer parallel to a first direction, each of the plurality of conductive lines are electrically coupled to each other;

wherein the conductive grid comprises:

a first conductive line of the plurality of conductive lines having a first width;

a second conductive line of the plurality of conductive lines having a second width, the second conductive line is spaced from the first conductive line in a second direction from the first conductive line, the second direction being perpendicular to the first direction, the second width being less than the first width;

a third conductive line of the plurality of conductive lines having a third width, the third conductive line is spaced from the second conductive line in the second direction from the second conductive line, the third width being greater than the second width, the second conductive line between the first and third conductive lines;

a fourth conductive line of the plurality of conductive lines having a fourth width, the fourth conductive line is spaced from the third conductive line in the second direction from the third conductive line, the fourth width being less than the third width, the third conductive line between the second and fourth conductive lines; and

a fifth conductive line of the plurality of conductive lines having a fifth width, the fifth conductive line is spaced from the fourth conductive line in the second direction from the fourth conductive line, the fifth width being greater than the fourth width, the fourth conductive line between the third and fifth conductive lines.

Referring to **claim 2**, Buffet further discloses that (From fig. 5) the first width, the third width, and the fifth width are the same width.

Referring to **claim 3**, Buffet further discloses that (From fig. 5) the second width and the fourth width are the same width.

Referring to **claim 4**, Buffet further discloses that (From fig. 5) the first width, the third width, and the fifth width are the same width; and the second width and the fourth width are the same width.

Referring to **claims 5-6, 7-9, and 11**, Buffet further discloses a sixth through thirteenth conductive lines as claimed, with the conductive lines being labeled as, from top to bottom of Fig. 6, first, sixth, tenth, second (two consecutive lines), eleventh, seventh, third, eight, twelfth, fourth (two consecutive lines), thirteenth, ninth, and fifth conductive lines.

Referring to **claim 10**, Buffet discloses in Fig. 6 an integrated circuit as claimed and as detailed above including the first through the thirteenth conductive lines, but fails to disclose explicitly in the figures a fourteenth through seventeenth conductive lines. However, as shall be apparent to one in the art, the Buffet's figures are only illustrative and not limiting, and full disclosure of the repetitive nature of the conductive lines can be found in the last paragraph of the description and in the claims, particularly claim 1.

Referring to **claims 12-13**, Buffet's Fig. 6 depicts a sixth through tenth conductive lines as claimed, with the eight conductive line being the center line 28', the sixth and tenth being the two outermost 28', and the seventh and ninth being between the respective outermost and center lines.

Referring to **claim 14**, the conductive lines are electrically connected together as claimed through vias such as 36.

Referring to **claim 15**, Buffet further discloses a plurality of conductive terminals (12') overlying the interconnect, the plurality of conductive terminal being positioned at a first pitch in the second direction, wherein a distance between a center of the first conductive line and a center

of the third conductive line is equal to the first pitch, wherein a distance between a center of the third conductive line and a fifth conductive line is equal to the first pitch.

Referring to **claim 16**, Buffet's Fig. 6 further depicts that a center of each conductive line of the plurality is located at a first distance from a center of an immediately adjacent conductive line of the plurality.

Referring to **claim 17**, Buffet further discloses a first signal line ("signal and I/O wiring") including at least a portion located between the first conductive line and the second conductive line in the interconnect layer (column 4, lines 40-45).

Referring to **claim 18**, Buffet's Figs. 2 and 6 further depict that each of the plurality of conductive lines extends across at least a substantial majority of the integrated circuit in the first interconnect layer parallel to the first direction.

Referring to **claim 19**, Buffet, as cited above, further discloses that each of the conductive lines of the plurality have a uniform width along at least a substantial majority of the integrated circuit.

Referring to **claims 20 and 21,** Buffet further discloses that the conductive grid is biased to provide a non-ground voltage ("power") or a ground voltage (column 5, first paragraph).

Referring to independent **claim 23** and using the same reference characters and citations as detailed above where applicable, and, to be consistent with claim terminology, from Fig. 5 of the Buffet's reference, the two center lines 30' being labeled as a second group of conductive lines, the two lines 30' most adjacent to the two center lines as a fourth group of conductive lines, the next two lines in the outward direction as a third group of conductive lines, and the

outermost lines 30' as a first group of conductive lines, Buffet discloses in effect an integrated circuit comprising:

a substrate including active circuitry;

an interconnect overlying the substrate; and

a conductive grid, the conductive grid including a plurality of conductive lines located in a first interconnect layer of the interconnect, each of the plurality of conductive lines extending across at least a substantial majority of the integrated circuit in the first interconnect layer parallel to a first direction, each of the plurality of conductive lines are electrically coupled to each other, each of the electrically conductive lines have a uniform width;

wherein the plurality of conductive lines includes a first group with each conductive line of the first group having a first width;

wherein the plurality of conductive lines includes a second group with each conductive line of the second group having a second width, the first width is greater than the second width;

wherein each conductive line of the second plurality is located between two lines of the first plurality;

wherein the plurality of conductive lines includes a third group with each conductive line of the third group having a third width;

wherein the third width is less than the first width and greater than the second width; and

wherein each line of the second group is located between two lines of the third group with no lines of the first group located there between.

Referring to **claim 24**, Buffet further discloses that the plurality of conductive lines includes a fourth group with each conductive line of the fourth group having a fourth width, the

fourth width is less than the third width and greater than the second width, each line of the second group is located between two lines of the fourth group with no lines of the first group located there between.

Referring to **claim 25**, Buffet further discloses that each line of the second group is located between two lines of the fourth group with no lines of the first group or the third group located there between.

Referring to **claims 26 and 27**, Buffet discloses in the figures an integrated circuit as claimed and as detailed above including the first, second, third, and fourth group of conductive lines but fails to disclose explicitly in the figures a fifth group of conductive lines. However, as shall be apparent to one in the art, the Buffet's figures are only illustrative and not limiting, and full disclosure of the repetitive nature of the group of conductive lines can be found in the last paragraph of the description and in the claims, particularly claim 1.

Referring to **claim 28**, Buffet further discloses that:

the conductive grid includes a second plurality of conductive lines (28') located in a second interconnect layer of the interconnect, each of the plurality of conductive lines extending across at least a substantial majority of the integrated circuit in a second interconnect layer parallel to a second direction, the second direction is perpendicular to the first direction, each of the second plurality of conductive lines are electrically coupled to each other and to each of the plurality of conductive lines, each of the second plurality of conductive lines have a uniform width;

the second plurality of conductive lines includes a fourth group (for example, the two conductive lines most adjacent to the two center conductive lines 28') with each conductive line of the fourth group having a fourth width;

the second plurality of conductive lines includes a fifth group (the two center conductive lines 28') with each conductive line of the fifth group having a fifth width, the fourth width is greater than the fifth width; each conductive line of the fifth plurality is located between two lines of the fourth plurality.

As for independent **claim 29**, Buffet discloses - with the same reference characters and citations as detailed above applied where applicable, and, to be consistent with claim terminology, from Fig. 6 of the Buffet's reference, the center lines 30' being labeled as a fifth conductive line, the two lines 30' most adjacent to the center line as a fourth and sixth conductive lines, the next two lines in the outward direction as a third and seventh conductive lines, the outermost lines 30' as a first and ninth conductive lines, and the two lines most adjacent to the outermost lines as a second and eight conductive lines - in effect an integrated circuit comprising:

a substrate including active circuitry;

an interconnect overlying the substrate; and

a conductive grid, the conductive grid including a plurality of conductive lines located in a first interconnect layer of the interconnect, each of the plurality of conductive lines extending across at least a majority of the integrated circuit in the first interconnect layer parallel to a first direction, each of the plurality of conductive lines are electrically coupled to each other;

wherein:

a first conductive line of the plurality of conductive lines has a first width;

a second conductive line of the plurality of conductive lines having a second width, the second conductive line is spaced from the first conductive line in a second direction from the first conductive line, the second direction being perpendicular to the first direction, the second width being less than the first width;

a third conductive line of the plurality of conductive lines having a third width, the third conductive line is spaced from the second conductive line in the second direction from the second conductive line, the third width being less than the second width, the second conductive line between the first and third conductive lines;

a fourth conductive line of the plurality of conductive lines having a fourth width, the fourth conductive line is spaced from the third conductive line in the second direction from the third conductive line, the fourth width being greater than the third width, the third line between the second and fourth conductive lines;

a fifth conductive line of the plurality of conductive lines having a fifth width, the fifth conductive line is spaced from the fourth conductive line in the second direction from the fourth conductive line, the fifth width being greater than the fourth width, the fourth conductive line between the third and fifth conductive lines;

a sixth conductive line of the plurality of conductive lines having a sixth width, the sixth conductive line is spaced from the fifth conductive line in the second direction from the fifth conductive line, the sixth width being less than the fifth width, the fifth conductive line between the fourth and sixth conductive lines;

a seventh conductive line of the plurality of conductive lines having a seventh width, the seventh conductive line is spaced from the sixth conductive line in the second direction from the sixth conductive line, the seventh width being less than the sixth width, the sixth conductive line between the seventh and fifth conductive lines;

an eighth conductive line of the plurality of conductive lines having an eighth width, the eighth conductive line is spaced from the seventh conductive line in the second direction from the seventh conductive line, the eighth width being greater than the seventh width, the seventh conductive line between the eighth and sixth conductive lines; and

a ninth conductive line of the plurality of conductive lines having a ninth width, the ninth conductive line is spaced from the eighth conductive line in the second direction from the eighth conductive line, the ninth width being greater than the eighth width, the eighth conductive line between the seventh and ninth conductive lines.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claim 22** is rejected under 35 U.S.C. §103(a) as being unpatentable over Buffet in view of Taylor et al. U.S. Patent 6,727,597.

Buffet discloses an integrated circuit substantially as claimed and as detailed above including the conductive grid 108 comprising the plurality of conductive lines for providing a

first voltage ("power") as claimed, but fails to disclose a second conductive grid for providing a second voltage different from the first voltage, i.e., ground potential, and including a second plurality of conductive lines comprising a sixth conductive line, and further fails to exactly disclose a seventh through tenth conductive lines as claimed. However, Buffet discloses in Figs. 1A, 5-6, and column 5, first paragraph that "[A] similar repeatable grid (not shown) for the ground bus may also be provided among corresponding ground contacts 14' (FIG. 1). Nevertheless, this teachings, together with Figs. 1A and 5-6, appears to disclose alternating power grids rather than alternating (and respective two adjacent conductive lines having the same width) power and ground arrangement, as elaborately recited in the claims.

Taylor, in disclosing a power arrangement for integrated circuits, teaches in column 3, lines 25-34, that by arranging ground bus 362 adjacent to power bus 360, inductance created by the opposing currents in the adjoining ground and power bus cancels most of the self inductance of these currents, and in addition, the power and ground bus arrangement reduces the horizontal inductance resistance drop between the respective power and ground buses.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Buffet's integrated circuit so that it comprises all limitations as claimed. One would have been motivated to make such a modification in view of the teachings by Taylor that by arranging ground bus adjacent to power bus, inductance created by the opposing currents in the adjoining ground and power bus cancels most of the self inductance of these currents, and in addition, the power and ground bus arrangement reduces the horizontal inductance resistance drop between the respective power and ground buses. Such a modification would create the sixth through tenth conductive lines as recited in claims 1 and 22.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 5,145,800 to Arai et al. discloses a method for providing a power grid for an integrated circuit by providing a power mesh wherein the width of each conductor and the distance between adjacent conductors are individually determined as demanded by circuit load.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
December 17, 2004